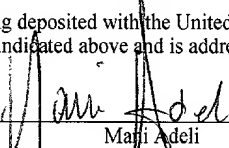


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Mari Adeli

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of:

Steven Teig, et al.

Serial No.: Not Yet Assigned

Filed: Herewith

For: **Integrated Circuit Wiring Architectures  
To Support Independent Designs (As  
Amended)**

**PRELIMINARY AMENDMENT**

Box PATENT APPLICATION  
Assistant Commissioner of  
Patents and Trademarks  
Washington, D.C. 20231

Sir:

This Preliminary Amendments is concurrently filed with the above-entitled application, which is a continuation application of a presently pending application entitled "Multi-Directional Wiring On A Single Metal Layer," filed on December 6, 2000.

**Applicants respectfully request that claims 1-15 be canceled (pursuant to the amendment below) before calculation of the filing fee.**

## IN THE TITLE

Please replace the current title, "Multi-Directional Wiring On A Single Metal Layer" with "Integrated Circuit Wiring Architectures To Support Independent Designs."

## IN THE SPECIFICATION

On page 1, line 1, please insert--

### Cross Reference to Related Applications

This application is a continuation application of United States Patent Application entitled " Multi-Directional Wiring On A Single Metal Layer " filed on December 6, 2000, and having the Serial No. \_\_\_\_\_.

On page 2, line 13 – page 4, line 8, please delete the “Summary of the Invention”, and insert therein a new Summary of the Invention as follows:

### SUMMARY OF THE INVENTION

An integrated circuit employs diagonal wiring geometries to provide noise immunity from Manhattan wiring geometries. Diagonal wires are routed over pre-configured or pre-designed blocks. The pre-configured blocks consist of self-contained sections within one or more metal layers of the integrated circuit, and implement Manhattan wiring geometries. The pre-configured blocks are not affected by the diagonal wires deposited on metal layers above them. The pre-configured blocks may include a memory, small cells that implement simple logic

functions, as well as large functional blocks that implement specific functionalities.

### **IN THE CLAIMS**

Please cancel claims 1-15, and add new claims 16-39 as follows:

16. (New) An integrated circuit comprising:

a plurality of metal layers comprising a plurality of conductors to interconnect components in said integrated circuit, said metal layers comprising:

a first metal layer group comprising at least one metal layer, said metal layer in said first metal layer group comprising at least one self contained layout section comprising conductors deposited in a preferred Manhattan direction, wherein a preferred direction defines a direction, relative to the integrated circuit boundaries, for at least fifty percent of conductors; and

a second metal layer group comprising at least one metal layer, said metal layer in said second metal layer group comprising a plurality of conductors deposited in a preferred diagonal direction in a portion of the metal layer directly adjacent to said self contained layout.

17. (New) The integrated circuit as set forth in claim 16, wherein said self contained layout section is independent of a layout for said second metal layer group.

18. (New) The integrated circuit as set forth in claim 16, further comprising a plurality of self contained layout sections in said first metal layer.

19. (New) The integrated circuit as set forth in claim 18, wherein at least one of said self contained layout sections comprise a wiring direction perpendicular to a wiring direction of a second one of said self contained layout sections.

20. (New) The integrated circuit as set forth in claim 16, wherein said self contained layout section comprises an entire one of said metal layer in said first metal layer group.

21. (New) The integrated circuit as set forth in claim 16, wherein said first metal layer group comprises three metal layers.

22. (New) The integrated circuit as set forth in claim 21, wherein said three metal layers each comprise conductors deposited in preferred Manhattan directions, wherein:

said first metal layer comprises a preferred Manhattan direction complementary of a preferred Manhattan direction of said second metal layer; and

said second metal layer comprises a preferred Manhattan direction complementary of a preferred Manhattan direction of said third metal layer.

23. (New) The integrated circuit as set forth in claim 16, wherein said diagonal direction comprises a direction 45 degrees relative to said integrated circuit boundaries.

24. (New) The integrated circuit as set forth in claim 16, wherein said diagonal direction comprises a direction 60 degrees relative to said integrated circuit boundaries.

25. (New) The integrated circuit as set forth in claim 16, wherein said self contained layout comprises a layout for a memory block.

26. (New) The integrated circuit as set forth in claim 16, wherein said self contained layout comprises a layout with a design independent from said layout of said second metal layer group.

27. (New) The integrated circuit as set forth in claim 16, wherein said self contained layout section comprises a section less than 10 percent of the entire area of said metal layer.

28. (New) A method for depositing a plurality of metal layers comprising a plurality of conductors to interconnect components of an integrated circuit, said method comprising the steps of:

designating a first metal layer group comprising at least one metal layer, said metal layer in said first metal layer group comprising at least one self contained layout section comprising conductors deposited in a preferred Manhattan direction, wherein a preferred direction defines a direction, relative to the integrated circuit boundaries, for at least fifty percent of conductors; and

designating a second metal layer group comprising at least one metal layer, said metal layer in said second metal layer group comprising a plurality of conductors deposited in a preferred diagonal direction in a portion of the metal layer directly adjacent to said self contained layout.

29. (New) The method as set forth in claim 28, wherein said self contained layout section is independent of a layout for said second metal layer group.

30. (New) The method as set forth in claim 28, further comprising a plurality of self contained layout sections in said first metal layer.

31. (New) The method as set forth in claim 30, wherein at least one of said self contained layout sections comprise a wiring direction perpendicular to a wiring direction of a second one of said self contained layout sections.

32. (New) The method as set forth in claim 28, wherein said self contained layout section comprises an entire one of said metal layer in said first metal layer group.

33. (New) The method as set forth in claim 28, wherein said first metal layer group comprises three metal layers.

34. (New) The method as set forth in claim 33, wherein said three metal layers each comprise conductors deposited in preferred Manhattan directions, wherein:

said first metal layer comprises a preferred Manhattan direction complementary of a preferred Manhattan direction of said second metal layer; and

said second metal layer comprises a preferred Manhattan direction complementary of a preferred Manhattan direction of said third metal layer.

35. (New) The method as set forth in claim 28, wherein said diagonal direction comprises a direction 45 degrees relative to said integrated circuit boundaries.

36. (New) The method as set forth in claim 28, wherein said diagonal direction comprises a direction 60 degrees relative to said integrated circuit boundaries.

37. (New) The method as set forth in claim 28, wherein said self contained layout comprises a layout for a memory block.

38. (New) The method as set forth in claim 28, wherein said self contained layout comprises a layout with a design independent from said layout of said second metal layer group.

39. (New) The method as set forth in claim 28, wherein said self contained layout section comprises a section less than 10 percent of the entire area of said metal layer.



## REMARKS

This Preliminary Amendments is concurrently filed with the above-entitled application, which is a continuation application of a presently pending application entitled " Multi-Directional Wiring On A Single Metal Layer " filed on December 6, 2000. In this Preliminary Amendment, Applicants have changed the title of this application, inserted a reference to the related parent application, canceled claims 1-15, and added new claims 16-39. Accordingly, claims 16-39 are currently pending in this application.

Respectfully submitted,

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Dated: December 15, 2000

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